6725439

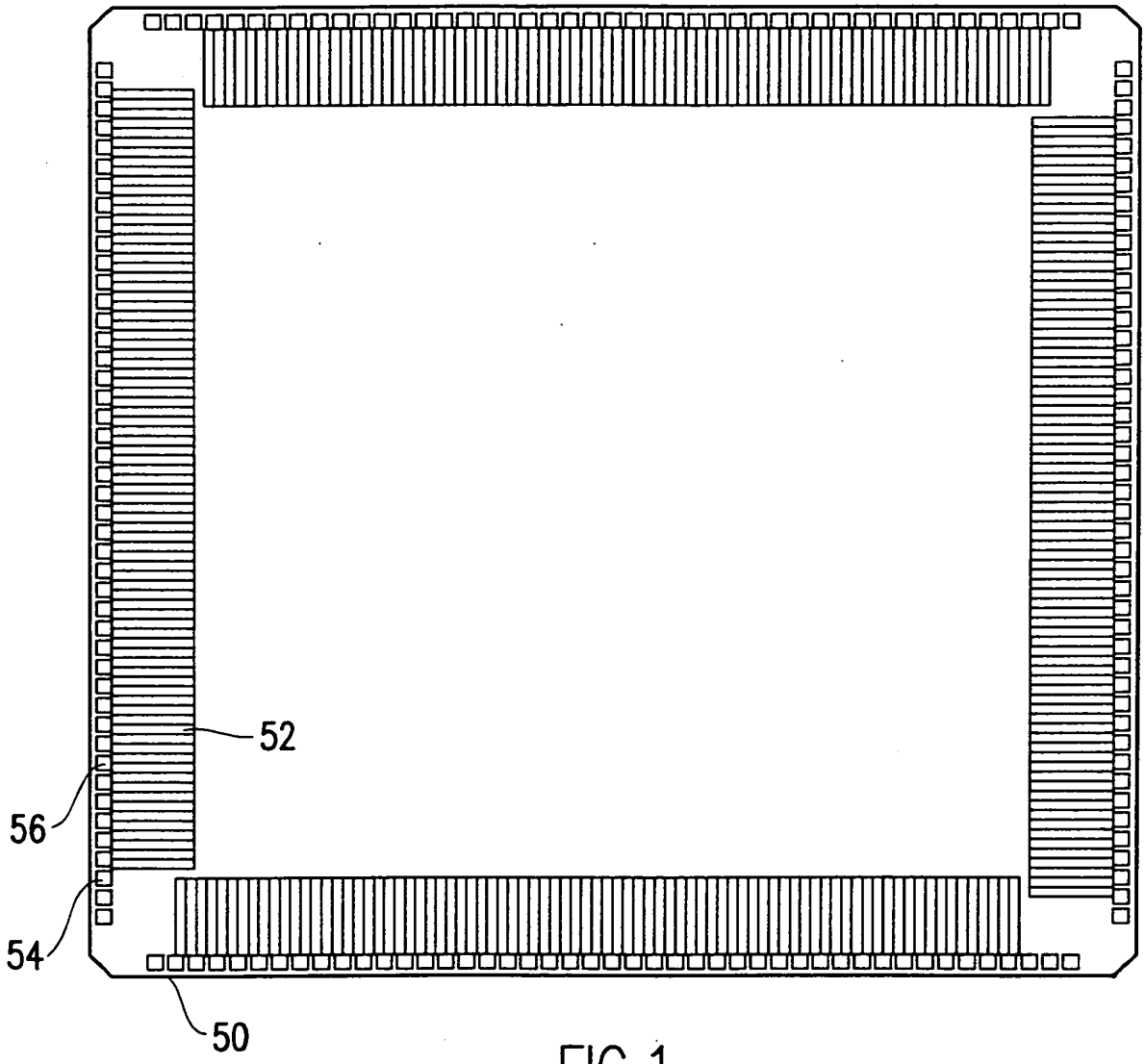

FIG. 1
PRIOR ART

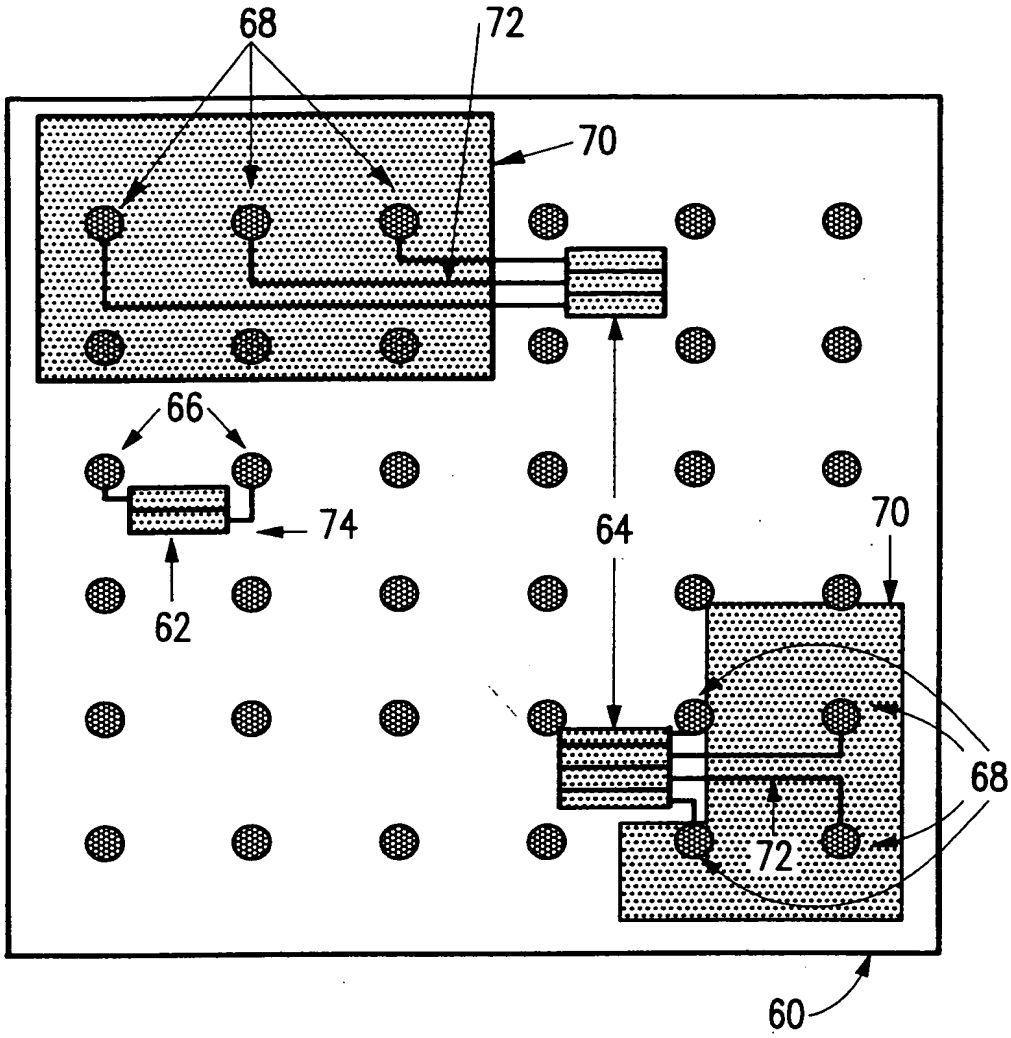

FIG.2

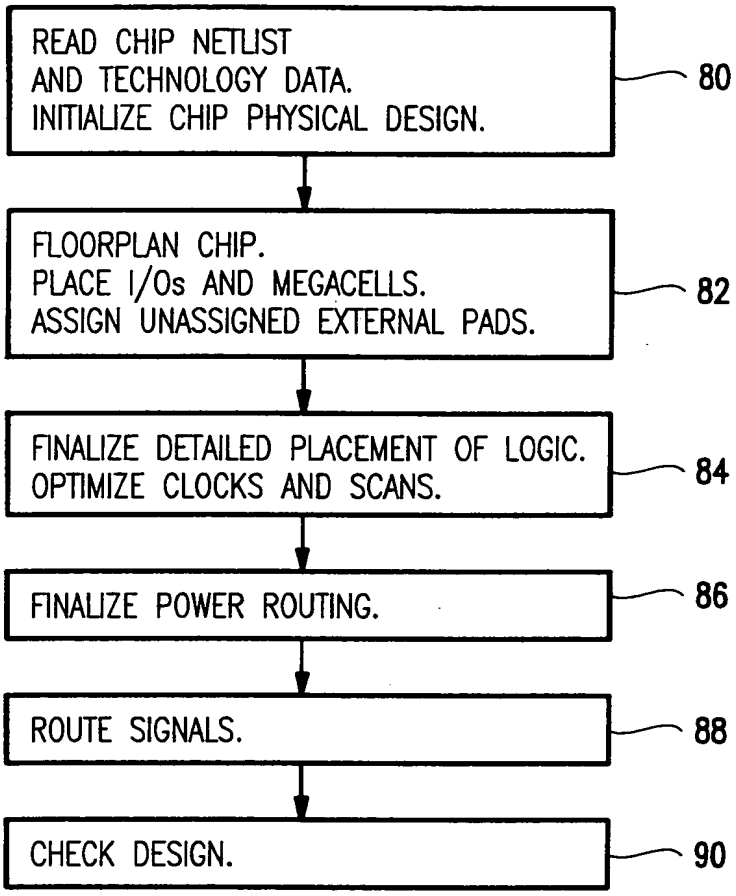
READ CHIP NETLIST
AND TECHNOLOGY DATA.
INITIALIZE CHIP PHYSICAL DESIGN.
80
FLOORPLAN CHIP.
PLACE I/Os AND MEGACELLS.
ASSIGN UNASSIGNED EXTERNAL PADS.
82
FINALIZE DETAILED PLACEMENT OF LOGIC.
OPTIMIZE CLOCKS AND SCANS.
84
FINALIZE POWER ROUTING.
86
ROUTE SIGNALS.
88
CHECK DESIGN.
90

FIG.3

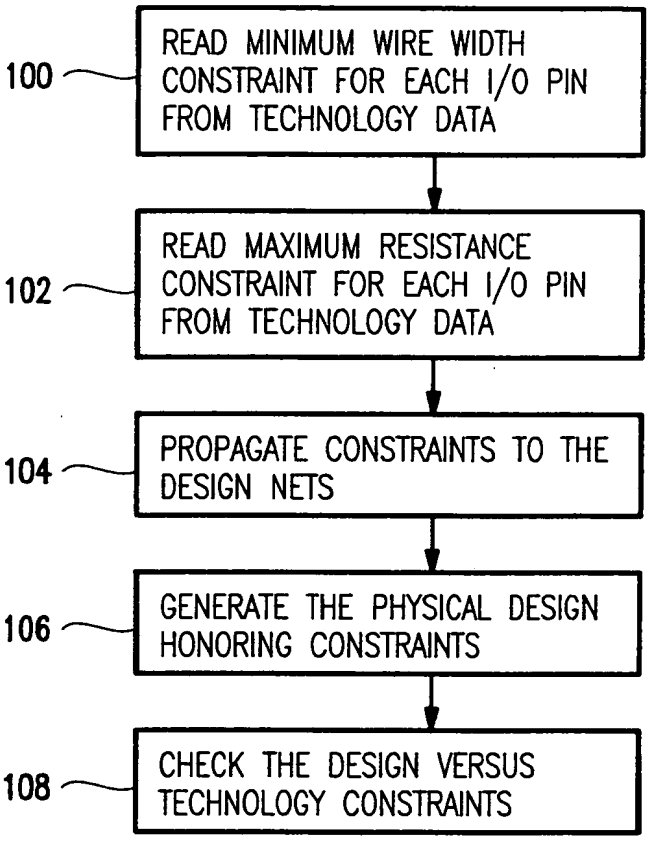
100
READ MINIMUM WIRE WIDTH CONSTRAINT FOR EACH I/O PIN FROM TECHNOLOGY DATA
102
READ MAXIMUM RESISTANCE CONSTRAINT FOR EACH I/O PIN FROM TECHNOLOGY DATA
104
PROPAGATE CONSTRAINTS TO THE DESIGN NETS
106
GENERATE THE PHYSICAL DESIGN HONORING CONSTRAINTS
108
CHECK THE DESIGN VERSUS TECHNOLOGY CONSTRAINTS

FIG.4

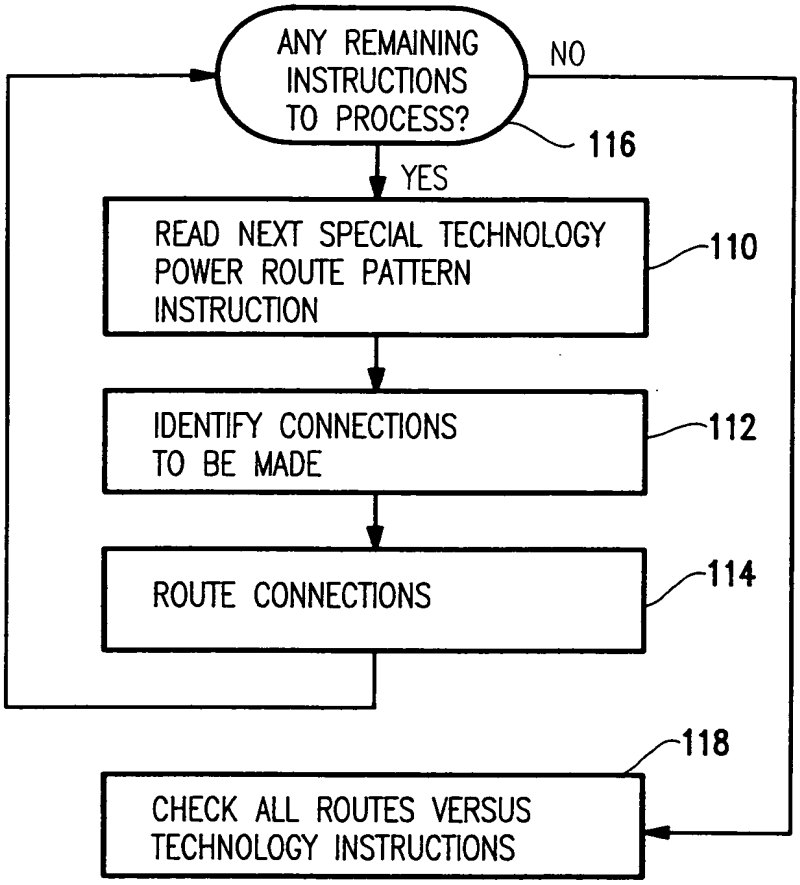
ANY REMAINING INSTRUCTIONS TO PROCESS?
NO
116
YES
READ NEXT SPECIAL TECHNOLOGY POWER ROUTE PATTERN INSTRUCTION
110
IDENTIFY CONNECTIONS TO BE MADE
112
ROUTE CONNECTIONS
114
118
CHECK ALL ROUTES VERSUS TECHNOLOGY INSTRUCTIONS

FIG.5

```
PowerPattern.GND_M4_UNUSED = {

        MiddleType      = UNUSEDPIN
        MiddleOwner     = CHIP
        MiddleLayer     = M5

        End1Type        = POWER
        End1Owner       = CHIP
        EndiLayer       = M5
        EndiProximity   = 2000  MICRON

        ConnectNet      = GND
        ConnectLayer    = M4
        ConnectWidt     = 16.3  MICRON
        ConnectSwath    = 58.1  MICRON
        ConnectAxis     = AXISVER
        }
```

FIG.6

```
PowerPattern.VDD_M4_ESD = {

        MiddleType      = PIN
        MiddleOwner     = ESD
        MiddleLayer     = M2
        MiddleStart     = (70.0 MICRON, 0.0 MICRON, LOWER_LEFT)
        MiddleEnd       = ( 0.0 MICRON, 0.0 MICRON, UPPER_RIGHT)
        MiddleAxis      = AXISVER
        Middleproximity = 180 MICRON


        End1Type        = POWER
        End1Owner       = CHIP
        End1Layer       = M5
        End1Proximity   = 2000 MICRON

        End2Type        = POWER
        End2Owner       = CHIP
        End2Layer       = M5
        End2proximity   = 2000 MICRON

        ConnectNet      = VDD
        ConnectLayer    = M4
        ConnectAxis     = AXISVER
        ConnectWidth    = 16.3 MICRON
        ConnectSwath    = 0 MICRON
        }
```

FIG.7

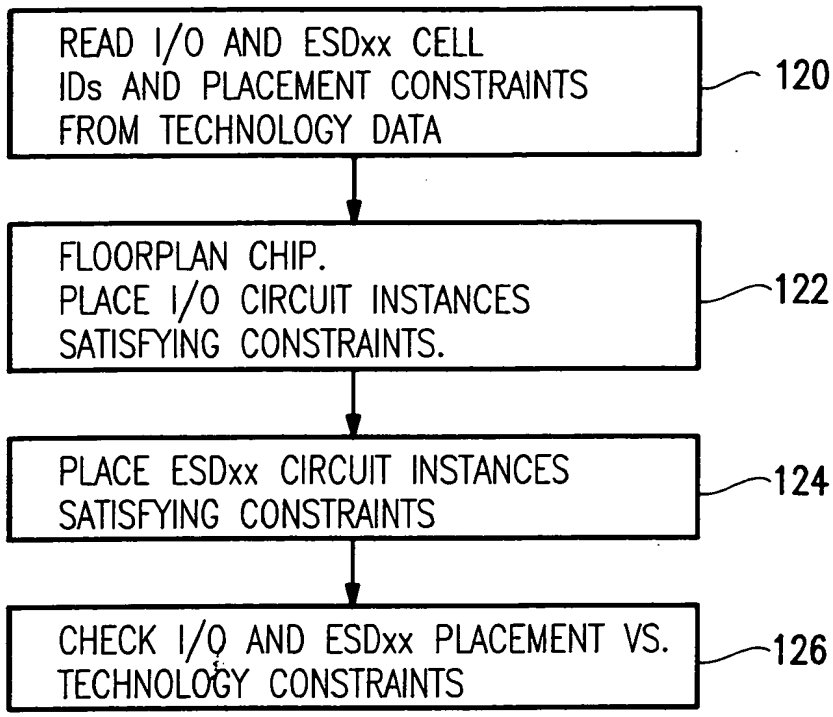
READ I/O AND ESDxx CELL IDs AND PLACEMENT CONSTRAINTS FROM TECHNOLOGY DATA
120
FLOORPLAN CHIP. PLACE I/O CIRCUIT INSTANCES SATISFYING CONSTRAINTS.
122
PLACE ESDxx CIRCUIT INSTANCES SATISFYING CONSTRAINTS
124
CHECK I/O AND ESDxx PLACEMENT VS. TECHNOLOGY CONSTRAINTS
126

FIG.8

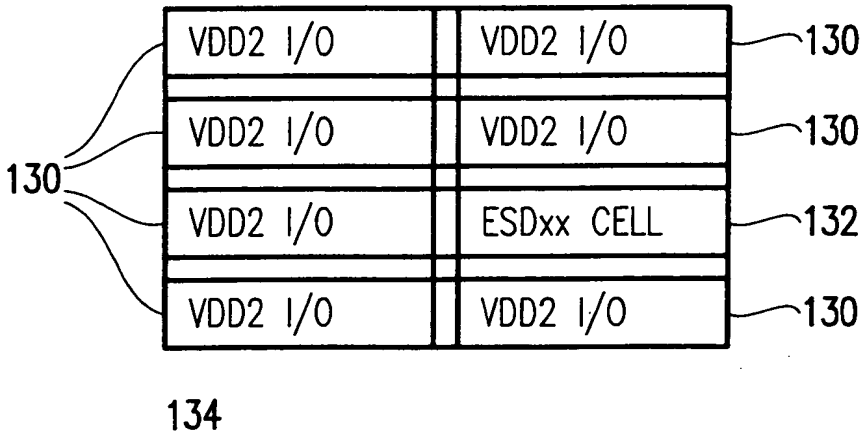
VDD2 I/O
VDD2 I/O
130
VDD2 I/O
VDD2 I/O
130
130
VDD2 I/O
ESDxx CELL
132
VDD2 I/O
VDD2 I/O
130
134

FIG.9